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Figs. 4A, 4B, and 4B are schematic views each showing voltage conditions of programming and erasion of a memory cell using the variable resistor element that is to be used in the present invention;

Fig. 5 is a flowchart of an erase method of the memory cell array configured by using the variable resistor elements that are to be used in the present invention;

Fig. 6 is a flowchart of an erase method of the memory cell array configured by using the variable resistor elements that are to be used in the present invention;

Fig. 7 is a configuration view showing another embodiment of a memory cell array section configured by using the variable resistor elements that are to be used in the present invention;

Fig. 8 is a block configuration view showing another embodiment of a memory cell array section configured by using the variable resistor elements that are used in the present invention;

Fig. 9 is a cross-sectional view of an ETOX type memory cell;

Fig. 10 is a configuration view of a source-common memory cell array section used in a conventional example; and

Fig. 11 is a flowchart showing a conventional example of an erase algorithm.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of a semiconductor memory device and an erase method for a memory cell array according to the present invention will be described with reference to the accompanying drawings.